

Amendments to the Specification

Please replace paragraph [0028] with the following paragraph:

--**FIG. 4A** illustrates how two PMOS transistors ~~301~~ 301A, 301B may be connected in parallel to achieve a relatively flat capacitance as a function of voltage V_g , which is illustrated by the solid line of **FIG. 4B**. The dashed lines of **FIG. 4B** are the individual $C(V_g)$ of the two devices ~~301~~ 301A, 301B of **FIG. 4A**. Note that in this case, with the use of two PMOS transistors ~~301~~ 301A, 301B, the C-V curve 404 is relatively flat, with a slight drop around zero volts. Thus, **FIG. 3B** shows the C-V curve for a single PMOS device, and **FIG. 4B** shows the C-V curves for two parallel-connected PMOS devices with opposite polarity. The C-V curve is symmetrical to $V_g=0$ and has dip around $V_g=0$. --